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Highly Linear and Symmetric Synaptic Memtransistors Based on Polarization Switching in Two-Dimensional Ferroelectric Semiconductors

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Brain-inspired neuromorphic computing hardware based on artificial synapses offers efficient solutions to perform computational tasks. However, the nonlinearity and asymmetry of synaptic weight updates in reported artificial synapses have impeded achieving high accuracy in neural networks. Here, this work develops a synaptic memtransistor based on polarization switching in a two-dimensional (2D) ferroelectric semiconductor (FES) of α-In_2Se_3 for neuromorphic computing. The α-In_2Se_3 memtransistor exhibits outstanding synaptic characteristics, including near-ideal linearity and symmetry and a large number of programmable conductance states, by taking the advantages of both memtransistor configuration and electrically configurable polarization states in the FES channel. As a result, the α-In_2Se_3 memtransistor-type synapse reaches high accuracy of 97.76% for digit patterns recognition task in simulated artificial neural networks. This work opens new opportunities for using multiterminal FES memtransistors in advanced neuromorphic electronics.

1. Introduction

The increasing demand in data collection and processing has boosted the implementation of artificial neural networks (ANNs) to tackle diverse problems, such as image recognition, natural language processing, and autonomous driving, inspired by the energy-efficient parallel processing capability of the human brain.[1–3] Because high power consumption is required to execute ANNs with complementary metal-oxide-semiconductor technology, neuromorphic hardware has drawn extensive interest to address the rapidly growing computation power and efficiency requirements.[4–7] One efficient approach is to develop high-performance artificial synapses capable of effectuating multilevel conductance states with high linearity and symmetry.[8,9] Compelling synaptic functions have been demonstrated in two-terminal memristors, while the inherently stochastic switching in most memristors inevitably causes nonlinear and asymmetry weight update issues that rapidly degrades ANN accuracy.[10–13] Meanwhile, memristors demand additional selecting circuitry components to reliably access and show limited synaptic tunability due to two-terminal device architecture, restricting further miniaturization and neuromorphic computing applications.[14–16] In this respect, memtransistor has risen as an outstanding multiterminal memristive device to circumvent existing limitations in memristors.[17–20] As a hybrid form of memristor and

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transistor, memtransistor can realize nondestructive reading and fine gate-tunable memristive switching behaviors. Particularly, two-dimensional (2D) polycrystalline MoS_2 based memtransistors have been extensively studied for nonvolatile memory and artificial synapses applications.[18,20–23] However, the resistive switching behaviors in reported memtransistors often relied on defects migration and/or charge trapping of randomly oriented grain boundaries, illustrating nonideal potentiation and depression synaptic profiles which could deteriorate the accuracy in neuromorphic computing.[24,25]

Ferroelectric (FE) materials have been used as outstanding artificial analog synapses with highly linear and symmetry synaptic weight update, because of the programmable polarization switching.[26,27] Previous work demonstrated that ferroelectric field-effect transistor (FE FET) with FE dielectric film reached greatly improved conductance tuning with low nonlinearity factors and a low asymmetry value, resulting in high online learning accuracy of 94.1% in ANNs.[26] Nevertheless, FE dielectrics often require stringent experimental conditions to stabilize the FE properties.[28] To this end, 2D van der Waals (vdW) ferroelectric semiconductors (FES), especially α-In_2Se_3, have drawn extensive interest in nonvolatile memories toward neuromorphic computing, because of their unique low-dimensional ferroelectricity with atomic thickness at room temperature and dangling-bond-free surface.[29–32] Despite important synaptic characteristics have been emulated in α-In_2Se_3 based synapses, their synaptic weight update is still inferior to aforementioned FE dielectric based counterparts, rendering them less advantageous in neuromorphic computing.[33,34]

Herein, we demonstrate a 2D FES synaptic memtransistor that can achieve near-ideal linearity and symmetry of synaptic characteristics essential for high-performance neural networks, by taking full advantage of fine-tunable FE polarization switching in α-In_2Se_3. The outstanding synaptic characteristics are achieved by the voltage-tunable Schottky barrier heights (SBHs) via the FE polarization switching in α-In_2Se_3 memtransistor, illustrating both electrically configurable long-term potentiation and depression (LTP/LTD) characteristics. The α-In_2Se_3 synaptic memtransistor exhibited superior linearity and symmetry in programmable conductance update, with nonlinearity factors of only 0.207 and 0.211 for potentiation and depression, near-ideal asymmetry value of 0.004, together with 100-level conductance states (more than 6 bits), outperforming reported artificial synapses based on FE dielectric and 2D FES transistors. As a result, the α-In_2Se_3 memtransistor-type synapse reached exceptionally high accuracies of 93.67%, 96.16%, and 97.76% for the Sandia file type, the University of California Irvine (UCI), and the Modified National Institute of Standards and Technology (MNIST) digit patterns in simulated ANNs, respectively. Our work opens new opportunities for using multiterminal FES memtransistors in advanced neuromorphic computing.

2. Results

2.1. Material Characterization of α-In_2Se_3

2D FES α-In_2Se_3 was theoretically and experimentally revealed the existence of in-plane (IP) and out-of-plane (OOP) ferroelectricity in ultrathin layers.[35–38] The α-In_2Se_3 used in this work was demonstrated to be *2H* crystal structure by Raman spectroscopy and X-ray diffraction (XRD) characterization. As shown in **Figure 1**a, the four Raman peaks at 90, 106, 187, and 194 cm^{-1}, assigned to be E^2, A_1(LO+TO), A_1(LO), and A_1(LO) phonon modes, respectively, are in accordance with typical values for α-In_2Se_3, and the peak at 90 cm^{-1} confirms the hexagonal structure.[35,39] In addition, the XRD pattern only displays *c*-plane peaks and high order interplanar spacing

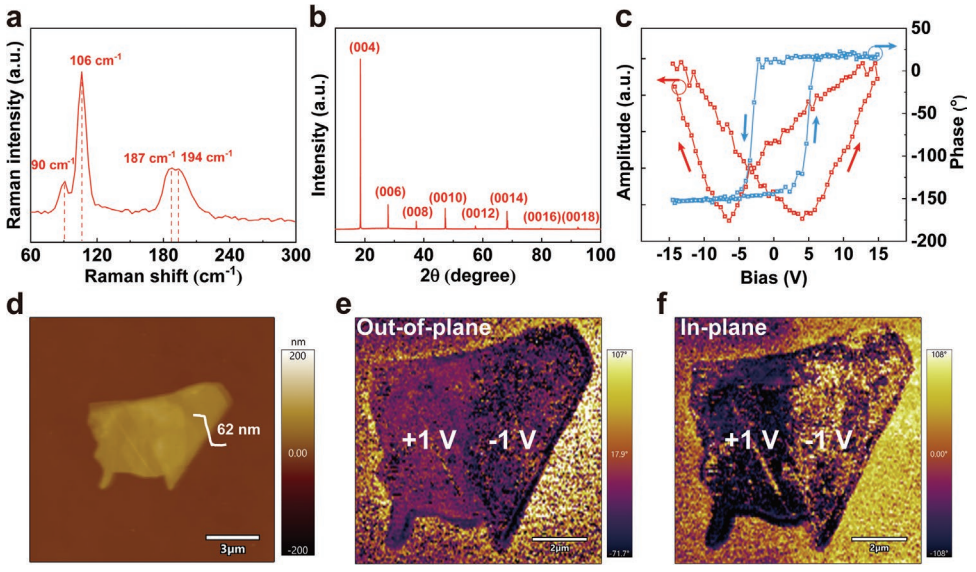

Figure 1. Material characterizations of α-In_2Se_3. a,b) Raman spectrum (a) and X-ray diffraction (XRD) spectrum (b) of the exfoliated α-In_2Se_3 flake, respectively. c) Off-field piezoelectric force microscopy (PFM) phase hysteresis (blue trace) and amplitude hysteresis loops (red trace) of a 120-nm-thick sample on Au-coated Si substrate, showing clear ferroelectric (FE) polarization switching of α-In_2Se_3 under external electric field. d) Atomic force microscopy (AFM) image of an exfoliated α-In_2Se_3 flake with a thickness of 62 nm. e,f) Out-of-plane PFM phase (e) and in-plane PFM phase (f) images of the polarized domain in α-In_2Se_3 flakes electrically written and measured by dual ac resonance tracking (DART) PFM, respectively.

corresponding to *2H* phase (Figure 1b), which is in line with previous reports.[39,40] In the crystal structure of *2H* α-In_2Se_3, each monolayer is composed of Se–In–Se–In–Se connected by covalent bonds (Figure S1, Supporting Information), while neighboring layers are bonded through weak vdW interactions.[37] The shift of the middle Se atom can reverse the orientation of quintuple layer, resulting in switchable polarization of the asymmetric arrangement, and fulfilling the symmetry breaking in ferroelectrics.[41,42]

The multilayer α-In_2Se_3 flakes were mechanically exfoliated and transferred onto substrate via polydimethylsiloxane (PDMS) films. To characterize the FE properties, we transferred a 120-nm-thick sample onto an Au-coated Si substrate, then performed the piezoelectric force microscopy (PFM) measurements. As shown in Figure 1c, both the off-field PFM amplitude and phase responses show hysteresis loops, indicating obvious FE polarization. Besides, the OOP and IP PFM phases and their corresponding amplitude images confirm the ferroelectricity (Figure S2, Supporting Information), where the phase indicates the direction of spontaneous polarization, and the amplitude reflects the magnitude of the local FE response. The strong piezoelectric signal with the phase-contrast difference of 180° can be observed, corresponding to two opposite polarization directions. These results verify the OOP and IP ferroelectricity of α-In_2Se_3 at room temperature. In addition, we characterized the atomic force microscopy (AFM) morphology and PFM images of a separate exfoliated flake with a thickness of 62 nm (Figure 1d). Figure 1e,f shows PFM phase images after applying opposite scanning voltages (±1 V) over different areas in the sample, resulting in distinguishable contrasts in both OOP and IP phase images, respectively, suggesting the FE polarization of α-In_2Se_3 can be switched electrically.

2.2. Electrical Performance of α-In_2Se_3 FES FET

Figure 2a shows the schematic diagram of α-In_2Se_3 FES FET with a bottom-gate top-contact configuration, with α-In_2Se_3 as FES channel, p^{++} Si substrate as gate electrode, 30-nm-thick Al_2O_3 as gate dielectric, and 3/50 nm thick Cr/Au as source/drain (*S*/*D*) electrodes. The false-color scanning electron microscopy (SEM) image (Figure 2b) presents a typical device with channel length (*L*) and width (*W*) of about 500 nm and 8 µm, respectively. The Al_2O_3 dielectric was grown by atomic layer deposition (ALD) at 175 °C (dielectric constant of 7.68, see Figure S3, Supporting Information). The Cr/Au *S*/*D* electrodes were defined by electron-beam lithography (EBL) and deposited by electron beam evaporation. Detailed device fabrication is provided in Experimental Section. Figure 2c presents the cross-sectional transmission electron microscopy (TEM) image and corresponding energy-dispersive X-ray spectroscopy (EDS) element mapping image of as-fabricated

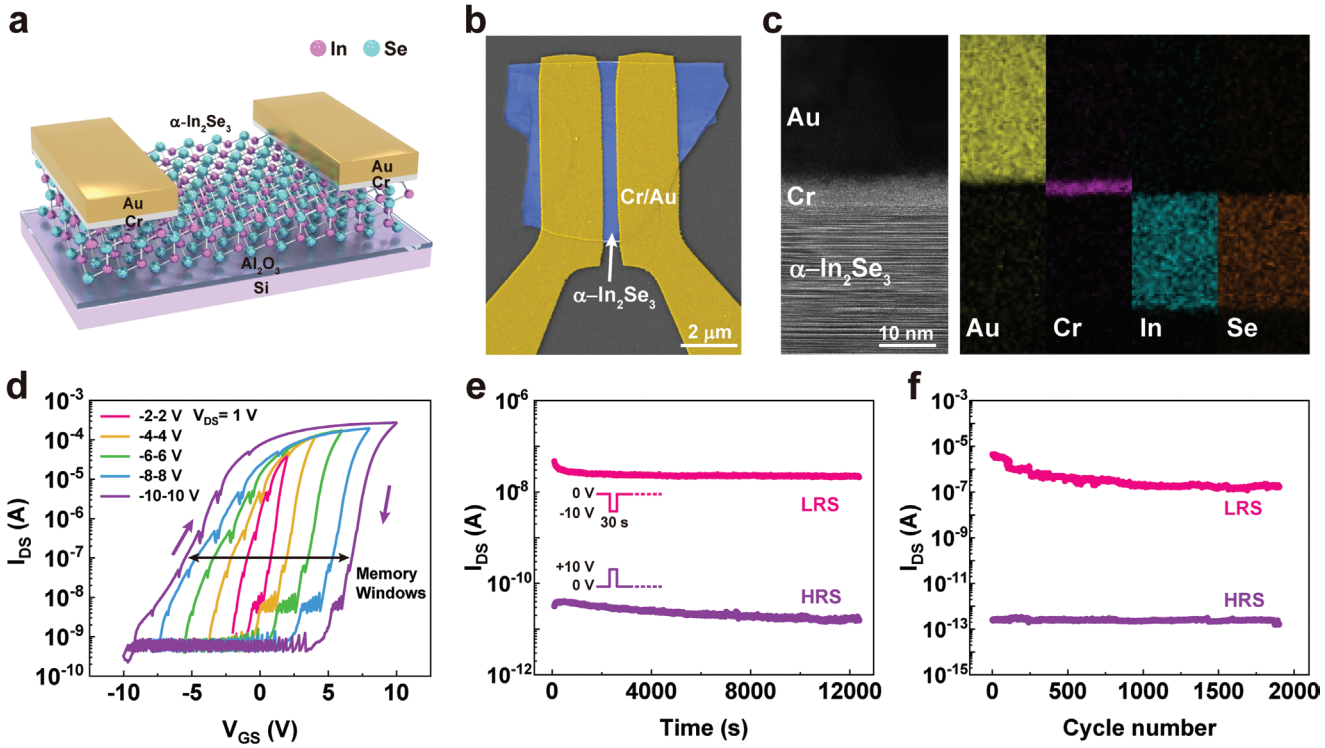

Figure 2. Structure and electrical performance of α-In_2Se_3 field-effect transistor (FET). a) Schematic diagram of α-In_2Se_3 FET with bottom-gate top-contact configuration, and ferroelectric semiconductor (FES) α-In_2Se_3 acted as the channel material. b) False-color scanning electron microscopy (SEM) image of the device. c) Cross-sectional transmission electron microscopy (TEM) image (left panel) and the corresponding chemical distribution of elements gold (Au), chromium (Cr), indium (In), and selenium (Se). d) Transfer characteristics of the α-In_2Se_3 FET at various gate voltage ranges measured with V_{DS} = 1 V. e) Retention characteristic of α-In_2Se_3 FET. The low resistance state (LRS) and high resistance state (HRS) currents were recorded at V_{DS} = 1 V, after V_{GS} write (–10 V, 30 s) and erase pulses (10 V, 30 s) at V_{DS} = 1 V, respectively. f) Endurance characteristic of α-In_2Se_3 FET. The LRS and HRS current values were extracted at V_{GS} = 0 V and V_{DS} = 1 V, from nearly 2000 consecutive closed-loop V_{GS} sweep cycles (between ±10 V) at V_{DS} = 1 V.

device, showing uniform metal-semiconductor contacts (Figure 2c, right).

Figure 2d shows representative transfer curves ($I_{DS} - V_{GS}$) of the device measured with different sweeping ranges of gate voltages at fixed source-drain voltage (V_{DS}) of 1 V. For the bottom-gate configuration, when a negative gate voltage is applied, positive polarization charges and electrons accumulate due to band bending, resulting in a low resistance state. In reverse, when a positive voltage is applied, negative polarization charges and holes are distributed, corresponding to the high resistance state.[43] By increasing the V_{GS} sweeping range, higher current on/off ratio ($I_{On/Off}$) of approximately 10^6 was achieved, indicating a high-quality oxide/semiconductor interface. In addition, the clockwise hysteresis loop is enlarged to achieve a large memory window with two different stable polarization states (Figure 2d), implying the accumulation of FE channel polarization can be regulated by the gate voltage. The maximum memory window of 12.4 V is achieved in V_{GS} sweeping ranges between ±10 V (Figure S4, Supporting Information). Because the hysteresis loops generated by defect trapping/detrapping are relatively small and sometimes even negligible, we could attribute the large clockwise hysteresis loops in the α-In_2Se_3 device mainly to the FE polarization switching, which is consistent with the previous reports.[30,43] To evaluate the uniformity, a statistics study on $I_{On/Off}$ of 51 devices with α-In_2Se_3 thicknesses in the range of 20–70 nm is depicted in Figure S5 (Supporting Information), showing a narrow device-to-device distribution.

We further investigated the retention performance of a separate α-In_2Se_3 device as a nonvolatile memory. Firstly, a close-looped V_{GS} sweep cycle (V_{GS} sweep from –10 to 10 V finally back to –10 V) at V_{DS} = 1 V was applied to eliminate any influence from previous applied voltages and set the device to an "initial" state. Secondly, a V_{GS} pulse (width: 30 s, amplitude: –10 V) was applied under V_{DS} = 1 V to program the device from "initial" state to and low resistance state (LRS). The LRS retention performance was then characterized by recording the LRS currents at V_{GS} = 0 V and V_{DS} = 1 V. Subsequently, a second consecutive close-looped V_{GS} sweep cycle (V_{GS} sweep from –10 to 10 V finally back to –10 V) at V_{DS} = 1 V was applied to set the device to the "initial" state again. A V_{GS} pulse (width: 30 s, amplitude: 10 V) was applied under V_{DS} = 1 V to erase the device from "initial" state to high resistance state (HRS). And the HRS retention performance was then characterized by recording the HRS currents at V_{GS} = 0 V and V_{DS} = 1 V. As shown in Figure 2e, the α-In_2Se_3 FET exhibits high retention performance (>12 000 s). In addition, we studied the endurance performance of α-In_2Se_3 FETs by applying consecutive closed-loop V_{GS} sweep cycles (V_{GS} sweep from –10 to 10 V and finally back to –10 V) at V_{DS} = 1 V. The LRS and HRS values were then extracted from different tested cycles at V_{GS} = 0 V and V_{DS} = 1 V (Figure 2f). The device showed stable performance for nearly 2000 test cycles. These results illustrate the high electrical performance of α-In_2Se_3 FES FETs as memory devices.

2.3. Tunable SBHs by FE Polarization Switching in α-In_2Se_3 Memtransistor

To study the electron transport mechanism in α-In_2Se_3 FES FET, we investigated the detailed current-voltage ($I_{DS} - V_{DS}$) characteristics. **Figure 3**a shows the $I_{DS} - V_{DS}$ curves with different V_{GS} plotted on a semilogarithmic scale. Despite with symmetric contact electrodes, the $I_{DS} - V_{DS}$ curves show asymmetric diodelike rectifying characteristics, indicating Schottky contacts formed at the metal–semiconductor interface. Importantly, the diodelike effect could be electrically configured by V_{GS} of different polarities. Under negative V_{GS} (–10 V), the device illustrates a positive rectifying behavior (Figure 3b, top panel). On the other hand, it changed to a negative rectifying behavior (Figure 3b, bottom panel) under positive V_{GS} (10 V). The gradual transition between bipolar rectifying behaviors could be attributed to the asymmetric modulation of the SBHs by FE polarization in α-In_2Se_3 (Figure S6, Supporting Information).[44] Figure 3c depicts the extracted the SBH values at different V_{GS} (Figure S6, Supporting Information), indicating that the SBHs at both *S* and *D* terminals decrease with V_{GS} changing from –10 to 10 V. Meanwhile, the SBHs decrease with increasing V_{DS} at fixed V_{GS}.

To understand the SBHs modulation mechanism, the energy band diagrams of α-In_2Se_3 FET at different operation stages are illustrated in Figure 3d–f. At original state (Figure 3d), the drain contact barrier height is higher than the source barrier according to measured *I*–*V* curve in Figure 3b (at V_{GS} = –10 V, top panel). When we applied forward voltage sweeping (V_{DS} sweeps from –1 to 1 V), the FE polarization pointed toward the source terminal and SBH gradually changed and finally switched. Correspondingly, a lower and higher barrier exists at the *D* and *S* terminals, respectively (Figure 3e), leading to opposite rectifying behavior at negative forward bias as shown in Figure 3b bottom panel. If we apply reverse voltage sweeping (V_{DS} sweeps from 1 to –1 V), the FE polarization will point toward the drain terminal again, resulting in higher SBH at drain terminal (Figure 3f). Such SBHs modulation behaviors were also observed in separate devices with different channel lengths (Figure S7, Supporting Information), confirming the high reliability due to FE polarization switching.

Based on the FE polarization correlated SBHs and the electrically configurable rectifying characteristics, the α-In_2Se_3 based FE memtransistor with multilevel resistance switching states is further elaborated.[45] A typical *I*–*V* characteristic without applying V_{GS} of α-In_2Se_3 FE memtransistors is shown in Figure 3g inset, with arrows and numbers denoting the sequence of voltage sweeps. Because the resistive switching is based on the FE polarization switching under external electric field, the device shows highly stable resistance switching characteristics during 30 repeated cycles. The energy band diagrams of the series current switching stages are illustrated in Figure S8 (Supporting Information). Importantly, gate voltage tunable memristive behaviors—critical characteristics of memtransistor—were enabled using a continuous sweep of V_{DS} range from –2 to 2 V under a series of V_{GS} (Figure 3g). Meanwhile, the hysteresis window of bipolar resistance switching can be tuned as a function of V_{GS}, resulting in wide gate-tunable multilevel resistance states. It is worth mentioning that the operating voltages (V_{DS}) of the α-In_2Se_3 memtransistor are in the range of ±2 V, which are lower than reported memtransistors.

To explore the nonvolatile resistance switching performance in α-In_2Se_3 memtransistor, we then studied the retention and endurance performance. We applied set (pulse amplitude:

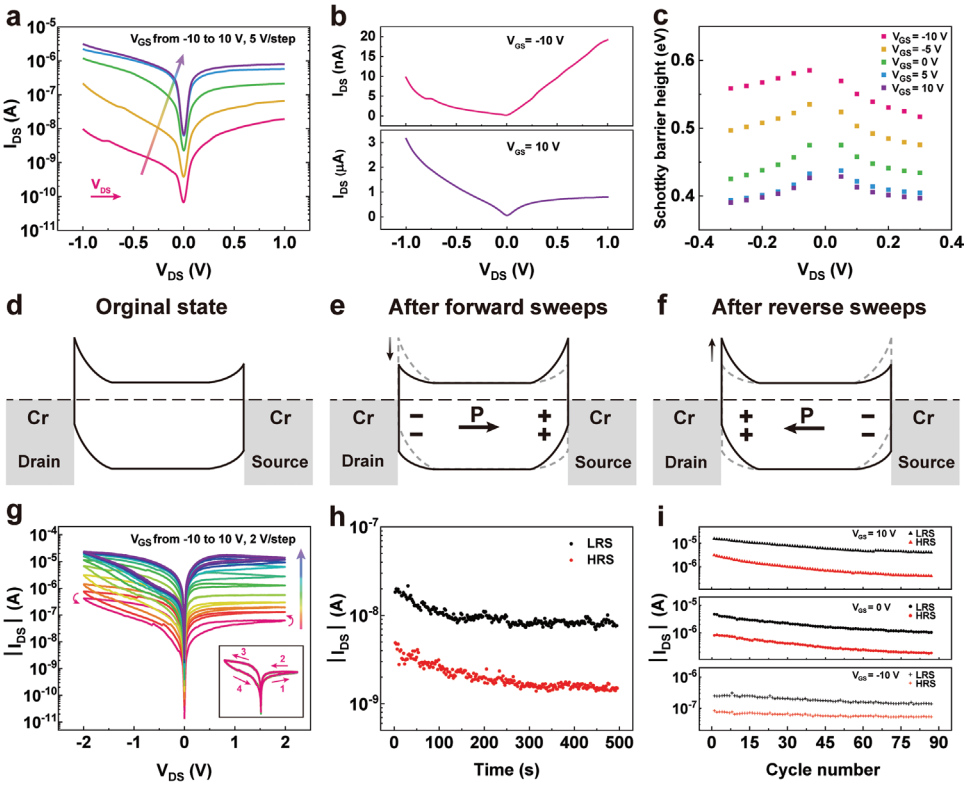

Figure 3. Tunable Schottky barrier heights by ferroelectric switching in ferroelectric semiconductor (FES) α-In_2Se_3 memtransistor. a) $I_{DS} - V_{DS}$ curves on semilogarithmic scales with different V_{GS} bias. The curves were measured on a forward sweep (from negative to positive voltages). b) Nonlinear diodelike $I_{DS} - V_{DS}$ curves on linear scales modulated at $V_{GS} = -10$ V (top panel) and $V_{GS} = 10$ V (bottom panel) bias. The data is extracted from (a). c) Extracted Schottky barrier height through the thermionic emission model in the range of sweep electric field with different gate voltages, the data is extracted from (a). d–f) Schematics of the energy band structure of drain and source terminals: at the defined original state (d), after V_{DS} forward sweeps (from negative to positive) at different gate voltages (solid line) (e), and after V_{DS} reverse sweeps (from positive to negative) at different gate voltages (solid line) (f). The dashed lines refer to the prior state in (e) and (f). g) $I_{DS} - V_{DS}$ curves of α-In_2Se_3 memtransistor with consecutive measurements over a V_{DS} range of –2 to 2 V, at different V_{GS} bias from –10 to 10 V with 2 V step^{-1}, exhibiting wide gate tunable conductance states. The inset shows $I_{DS} - V_{DS}$ curves of 30 consecutive V_{DS} sweep cycles measured at $V_{GS} = 0$ V. The direction of V_{DS} sweeps is indicated by arrows and numbers. h) Retention of the high resistance state (HRS) (after V_{GS} pulse = –2 V, V_{DS} pulse = –1 V, 20 s) and low resistance state (LRS; after V_{GS} pulse = +2 V, V_{DS} pulse = –1 V, 20 s) currents. The HRS and LRS current values were read at $V_{DS} = -0.1$ V and $V_{GS} = 0$ V. i) Endurance characteristics of α-In_2Se_3 memtransistor at different V_{GS} (10, 0, and –10 V, from top to bottom). The HRS and LRS current values are extracted at $V_{DS} = -1$ V from consecutive V_{DS} sweep cycles, illustrating the V_{GS}-configurable multilevel resistance states.

$V_{GS} = +2$ V, $V_{DS} = -1$ V, pulse width: 20 s) and reset (pulse amplitude: $V_{GS} = -2$ V, $V_{DS} = -1$ V, pulse width: 20 s) voltage pulses, and read the LRS and HRS currents at $V_{DS} = -0.1$ V and $V_{GS} = 0$ V, respectively (Figure 3h). It is noted that the HRS and LRS values show similar temporary decays, thus the $I_{On/Off}$ remains relatively unchanged for 500 s.

We then studied the endurance performance of the α-In_2Se_3 memtransistor by extracting LRS and HRS values at $V_{DS} = -1$ V from the $I_{DS} - V_{DS}$ curves in Figure 3g. Figure 3i shows the extracted LRS and HRS values at different $V_{GS} = 10$, 0, and –10 V (from top to bottom panels), illustrating the V_{GS}-configurable multilevel resistance states in α-In_2Se_3 memtransistor. Such wide gate-tunable multilevel conductance behaviors were also observed in separate devices (Figure S9, Supporting Information). The presented V_{GS} tunable resistance switching properties of FES are different with those based on grain-boundary-mediated migration of polycrystalline materials (Table S1, Supporting Information), which opens new opportunities for neuromorphic computing applications requiring multiterminal devices.

2.4. Configurable Synaptic Plasticity in α-In_2Se_3 Memtransistor

The configurable multilevel conductance states of the α-In_2Se_3 FES memtransistor pave the way for mimicking the multiple synaptic plasticity of biological counterparts (**Figure 4**a), and both V_{GS} and V_{DS} pulses can simulate presynaptic inputs and I_{DS} is monitored as postsynaptic current (PSC). Because linearity and symmetry of synaptic weight update are significant parameters to achieve high accuracy of various tasks performed by neural network simulations, we studied these characteristics of α-In_2Se_3 FES memtransistor under different V_{GS} and V_{DS} presynaptic pulse schemes. Detailed analysis on nonlinearity and asymmetry extraction is presented in Figure S10 (Supporting Information).

First, we investigated the influence of different V_{GS} on PSC characteristics at same V_{DS} bias. When an identical V_{GS} pulse scheme with constant pulse amplitude and width was used, the PSC responses showed poor potentiation/depression (P/D)

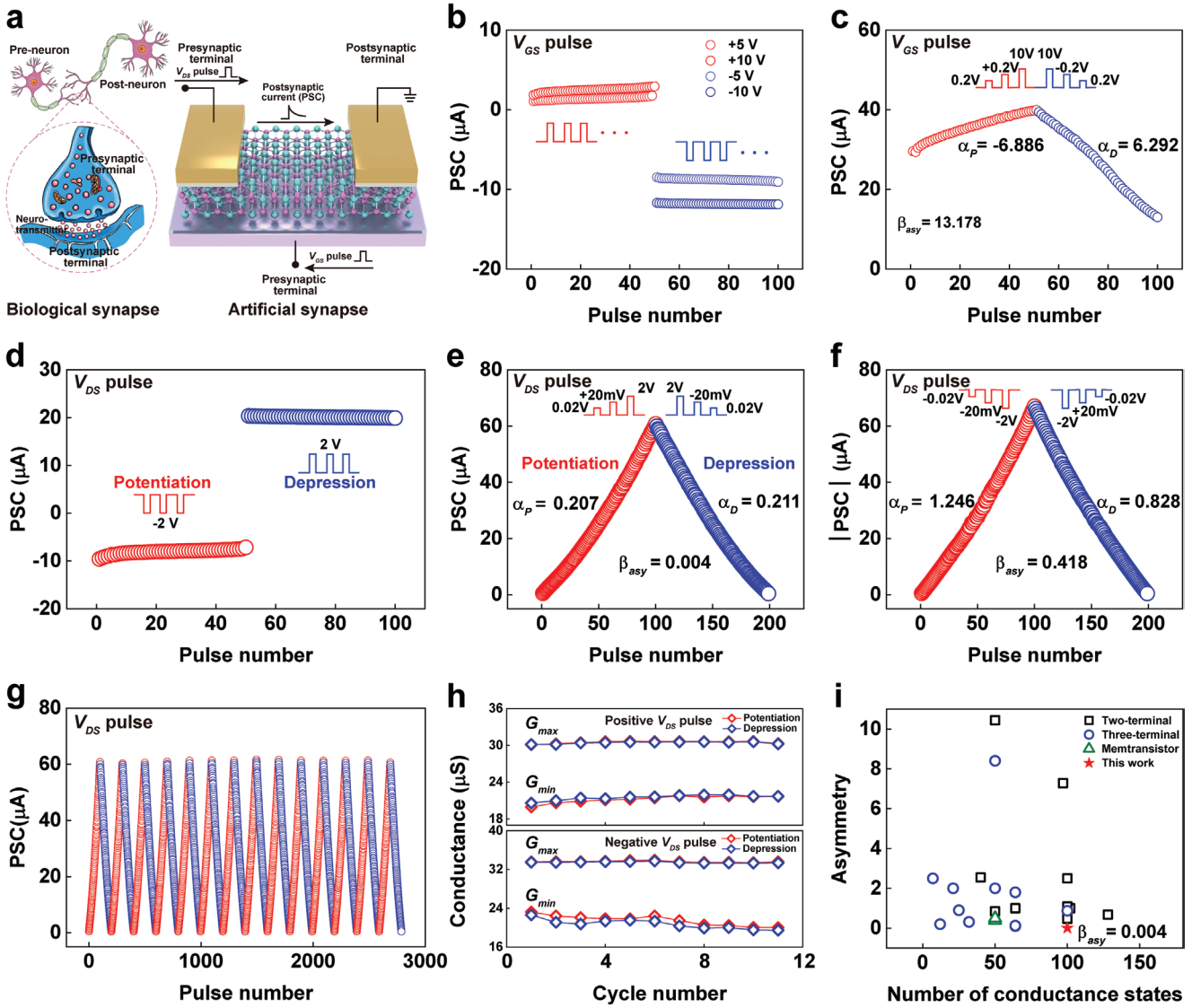

Figure 4. Configurable potentiation and depression characteristics in α-In_2Se_3 memtransistor-based artificial synapse under various voltage pulse schemes. a) Schematic illustration of biological neurons and synapses (left) and the α-In_2Se_3 memtransistor-based artificial synapse (right). The electrical pulses at gate or drain terminal (V_{GS} or V_{DS} pulse) both can served as presynaptic input, and I_{DS} is monitored as postsynaptic current (PSC). b) PSCs under identical V_{GS} pulse schemes (amplitude: ±5 V, ±10 V, width: 10 ms) at V_{DS} bias (1 V). c) PSCs under incremental and decremental positive V_{GS} pulse schemes (pulse width: 10 ms) at V_{DS} bias (1 V). d) PSCs under identical V_{DS} pulse schemes (amplitude: ±2 V, width: 30 ms) at V_{GS} bias (2 V). e,f) PSCs under nonidentical amplitude-modulated positive (e) and negative (f) V_{DS} pulse schemes at V_{GS} bias (2 V), showing excellent linearity and symmetry. g) Electrical stability analysis of the artificial synapse with a non-identical pulse scheme in (e) at V_{GS} = 2 V. h) Extracted G_{max} and G_{min} from the potentiation and depression characteristic curves in (e) (top panel) and Figure S15g (Supporting Information, bottom panel). i) Comparison of asymmetry values of synaptic weight update and number of conductance states of α-In_2Se_3 memtransistor-based synapse with reported counterparts. Asymmetry value of 0 indicates perfect symmetric characteristic.

characteristics (Figure 4b). Then we applied nonidentical, amplitude-modulated incremental/decremental (amplitude increases/decreases with constant value) positive and negative V_{GS} pulse schemes at different V_{DS}, the P/D behaviors were distributed in mismatched PSC levels which was unfavorable (Figure S11, Supporting Information). As depicted in Figure 4c, the P/D characteristics was improved under incremental/decremental positive V_{GS} pulses, showing nonlinearity factors of −6.886 for potentiation (α_P) and 6.292 for depression (α_D), and a large asymmetry value of 13.178 ($\beta_{asy} = |\alpha_P - \alpha_D|$). The P/D characteristics were further improved by applying incremental/decremental negative V_{GS} pulse schemes (Figure S12, Supporting Information). Still, these poor linear characteristic and limited number of available conductance states impeded the applications in neural networks. The inferior PSC characteristics could be attributed to the relatively thick (30 nm) Al_2O_3 dielectric layer, leading to less V_{GS}-configurable FE polarization in α-In_2Se_3.[44]

Then, we explored the P/D characteristics as a function of V_{DS} pulse schemes under the same V_{GS} bias. Figure 4d shows

the PSC responses obtained after 50 identically negative/positive (± 2 V) V_{DS} pulses at V_{GS} bias (2 V), exhibiting P/D characteristics, respectively, due to the V_{DS} induced IP FE polarization switching in FES α-In_2Se_3. Benefited from the short channel length (about 500 nm), the amplitude of V_{DS} pulse (within ±2 V) required for the conductance modulation was low, providing low voltage operations. However, the large mismatch in P/D conductance levels deteriorates the inference accuracy in neural networks.

To optimize the linearity and symmetry, we then carried out amplitude-modulated V_{DS} pulse schemes. Figure 4e,f depicts the corresponding excitatory and inhibitory PSC (EPSC/IPSC) characteristics, respectively. Programmable EPSC of P/D characteristics were realized by amplitude-modulated positive V_{DS} pulse scheme, where the amplitude of pulses increased from 0 to 2 V in a 20 mV step and decreased from 2 to 0 V in a −20 mV step (Figure 4e). Meanwhile, IPSC of P/D characteristics were obtained with amplitude-modulated negative V_{DS} pulse scheme, where V_{DS} amplitudes decreased from 0 to −2 V in a −20 mV and increased from −2 to 0 V in a 20 mV step (Figure 4f). In this way, the device showed highly linear, symmetric PSC responses and obtained 100-level conductance states (more than 6 bits) by nonidentical positive and negative V_{DS} pulse schemes (Figure 4e,f, and Figure S13, Supporting Information). More importantly, it exhibited near-ideal linearity of $\alpha_P = 0.207$ and $\alpha_D = 0.211$ ($\alpha_P = 1.246$, $\alpha_D = 0.828$), and asymmetry of $\beta_{asy} = 0.004$ ($\beta_{asy} = 0.418$) for EPSC (IPSC), outperforming previously reported artificial synapses based on FE dielectric and FES transistors. This highly linear and symmetry performance is more depended on V_{DS} modulation and is also attainable under different V_{GS} constant bias (Figure S14, Supporting Information). In this respect, we could effectively reshape the linearity and symmetry of synaptic weight update behaviors in FES memtransistors by facilely modulating V_{DS} pulse scheme, illustrating the advantages of FE polarization switching in constructing artificial synapses.

Furthermore, we investigated the endurance performance of the FES memtransistor by applying a series of P/D V_{DS} pulse cycles up to 2800 pulses with different V_{GS} bias (Figure 4g and Figure S15, Supporting Information). The device maintained excellent synaptic responses even after various test cycles, indicating the reliability of FE polarization switching. Meanwhile, the top and bottom panels in Figure 4h depict the maximum and minimum conductance values (G_{max} and G_{min}) extracted from the P/D curves under positive (Figure 4g) and negative (Figure S15g, Supporting Information) V_{DS} pulse schemes at same V_{GS} of 2 V, respectively. The attained G_{max} and G_{min} values maintained stable with approximately 30 (32) and 20 (23) μS for positive (negative) V_{DS} pulse schemes, respectively. As shown in Figure 4i, we compared the proposed FES synaptic memtransistor and documented artificial synapses in terms of the number of conductance states and asymmetry value of synaptic weight update. The asymmetry value of 0.004 achieved by our device outperforms those of synaptic counterparts with both two- and three-terminal devices. A more detailed comparison of synaptic performance with reported artificial synapses is presented in Table S2 (Supporting Information).

2.5. Implementation of Neuromorphic Computing Simulation

The highly linear and symmetric synaptic weight update characteristics render the α-In_2Se_3 FES memtransistor-based synapses feasible for high-accuracy neuromorphic computing. To demonstrate this, we implemented the FES synapses in neural network via back-propagation (BP) algorithms. As shown in **Figure 5**a, we defined a three-layer ANN, including input, hidden, and output neuron layers for pattern recognition. We used three datasets for simulation tasks: the Sandia file types data set, the UCI (8 × 8 pixel) data set, and the MNIST (28 × 28 pixel) handwritten digits data set (Table S3, Supporting Information).

The voltage signals (V_i) corresponding to each pixel of the patterns in different datasets were applied to the input neuron layer. Then they were multiplied by the synaptic weight ($W_{i,j}$) and consequently transformed to weight sum currents ($I_j = \sum_{i=1}^{i} W_{i,j} \times V_i$ for the *j-th* current in hidden layer). Next, the hidden voltage signals were obtained via the sigmoid activation function and experienced similar operation between two layers. Finally, the output value k was compared with each labeled value to calculate the error, and the synaptic weights were updated by minimizing the errors by the BP algorithm. The synaptic weight was predefined as the measured conductance parameters of α-In_2Se_3 memtransistor-based synapse ($W = G$), and each neuron in one layer was fully connected to all neurons in the next layer via the electronic synapse.

To elucidate the influence of linearity and symmetry of synaptic weight update on inference accuracy, we compared the simulation results based on artificial synapses configured by different V_{GS} and V_{DS} pulse schemes. Figure 5b shows the corresponding parameters of the electronic synapse under amplitude-modulated positive V_{GS} pulse schemes. We then condensed the P/D cycling results to analyze the write noise. Figure 5c,d unravels the cumulative distribution function (CDF) heat maps of potentiation and depression, respectively, which represent the degree of ΔG versus G, where G stands for each conductance state, and ΔG is the change conductance induced by write noise. The synapse configured by V_{GS} pulse scheme showed large conductance response variability, which may deteriorate the accuracy of ANNs. As a result, relatively low accuracies of 88.22%, 91.77%, and 92.55% were obtained after 40 training epochs for the file type, the UCI, and the MNIST datasets, respectively (Figure 5e). And the accuracies are much lower than that training using ideal numeric (Figure S16, Supporting Information). In comparison, based on synapses under amplitude-modulated negative V_{DS} pulse scheme, elevated accuracies of 93.44%, 95.88%, and 97.68% were obtained at the same conditions for the file type, the UCI, and the MNIST datasets, respectively (Figure S17, Supporting Information). Furthermore, we carried out the simulation with electronic synapse under amplitude-modulated positive V_{DS} pulse scheme, which exhibited the best near-ideal linear and symmetry conductance parameters (Figure 5f). Meanwhile, it demonstrates small conductance response variability of ≈0.1 μS in both potentiation (Figure 5g) and depression (Figure 5h) CDF heat maps. In result, the ANNs with the artificial synapse depicted superior accuracies of 93.67%, 96.16%, and 97.76%

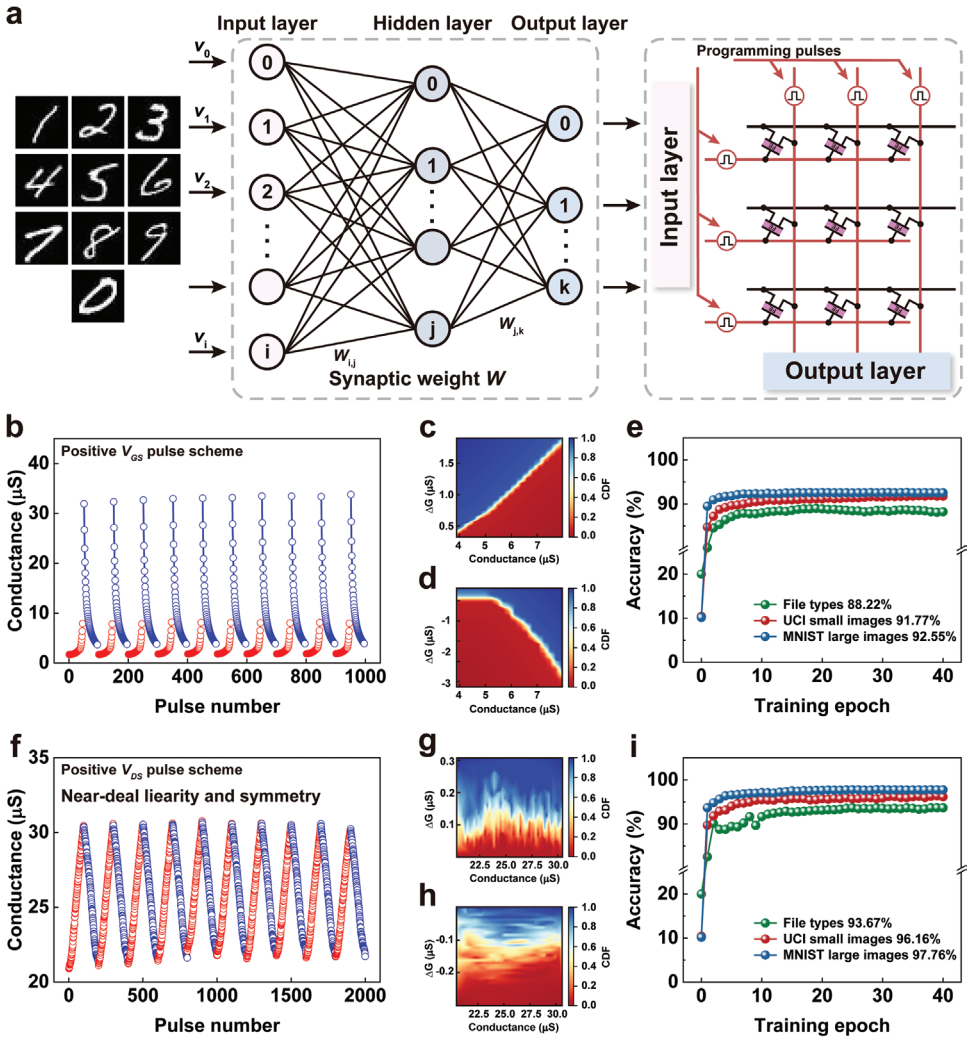

Figure 5. Implementation of neuromorphic computing simulation based on α-In_2Se_3 synaptic memtransistor. a) Schematic illustration of neural networks consisting of input neurons, hidden neurons, and output neurons (middle panel), and the circuits for α-In_2Se_3 synapses for the conceptual neural networks (right panel). b) Cycle-to-cycle variations of programmed conductance states in *P*/*D* curves for 10 cycles with nonidentical positive V_{GS} pulse scheme (Figure 4c), data extracted in Figure S12a (Supporting Information). c,d) Cumulative distribution function (CDF) heat maps representing ΔG as a function of *G* during potentiation (c) and depression (d) with data extracted in (b). e) The accuracy of α-In_2Se_3 synapses for different pattern recognition based on the conductance parameters in (b). f) Cycle-to-cycle variations of programmed conductance states in *P*/*D* curves for 10 cycles with nonidentical positive V_{DS} pulse scheme. g,h) CDF heat maps during potentiation (g) and depression (h) with data extracted in (f). i) The accuracy of α-In_2Se_3 synapses for different pattern recognition based on the conductance parameters in (f). The accuracies after 40 training epochs were presented.

after 40 training epochs for the file type, the UCI, and the MNIST datasets, respectively (Figure 5i). These results demonstrated the advantages of the α-In_2Se_3 memtransistor-based synaptic devices in neural networks, providing more configurable near-ideal linearity and symmetry, multilevel conductance states, and small conductance response variability characteristics, which are originated from the FE polarization switching in FES channel.

3. Conclusions

In conclusion, we have achieved 2D FES α-In_2Se_3 based synaptic memtransistors with near-ideal linearity and symmetry of synaptic weight update for hardware implementation of neuromorphic computing. The α-In_2Se_3 memtransistor exhibits gate-tunable SBHs by FE polarization switching, illustrating highly configurable conductance potentiation and depression characteristics via various voltage pulse schemes. Importantly, near-ideal linearity and symmetry weight update characteristics, with nonlinearity factor α_P = 0.207 and α_D = 0.211, and asymmetry value of only 0.004, together with 100-level conductance states (more than 6 bits), were achieved in α-In_2Se_3 synaptic memtransistor by amplitude-modulated V_{DS} pulse schemes, outperforming documented artificial synapses based on FE dielectric and 2D FES transistors. As a result, the α-In_2Se_3 synapse based ANNs reached outstanding accuracies of 93.67%, 96.16%, and 97.76% for the file type, the UCI small image, and the MNIST handwritten image datasets. These results open new opportunities for implementing FES

memtransistor configuration in realizing high-performance neuromorphic computing.

4. Experimental Section

Device Fabrication: The p^{++} Si wafers were cleaned by sequential ultrasonication in acetone, isopropanol, and deionized (DI) water for 10 min, then 30 nm Al_2O_3 layer as the dielectric layer was deposited by using $Al(CH_3)_3$ (TMA) and H_2O as precursors at 175 °C. The α-In_2Se_3 flakes were exfoliated from bulk crystals (purchased from HQ Graphene, purity >99.995%) onto the 30 nm Al_2O_3 on the Si substrate using Scotch tape. The exfoliation was performed in a glove box with nitrogen environment. The electrode pattern was defined by EBL (Raith 150 Two) using a 200 nm thick 950K A4 poly(methyl methacrylate) (PMMA) resist (baked at 180 °C for 90 s). EBL was performed on a lithography system at a dose of 300 μC cm^{-2} and an acceleration voltage of 30 kV, and then deposited by electron-beam evaporation. The electrode films as source and drain contacts were approximately Cr/Au 3 nm/30 nm. Finally, the device was immersed in hot acetone (50 °C) for 10 min to lift off.

Material Characterization: The crystallization information of exfoliated α-In_2Se_3 flakes was obtained using XRD (D8 Advance, Bruker). The Raman measurement was carried out on a WITec Alpha 300R Raman spectrometer with 532 nm laser excitation. The thickness of the exfoliated α-In_2Se_3 flakes was measured by AFM (Cypher ES, Oxford Instruments). PFM tests were examined by α-In_2Se_3 flakes on Au (30 nm)/Si substrate using Ti/Pt (5/20 nm) coated conductive tip (AC240TM, Olympus). The out-of-plane and in-plane piezoelectric signals were acquired at a contact resonance frequency of ≈260 kHz in DART (dual ac resonance tracking) PFM mode. The structure information was investigated by using TEM (JEOL JEM-F200). EDS elemental maps were used to show the continuous presence of Cr layer between the Au and α-In_2Se_3.

Electrical Characterization: The channel width (*W*) and length (*L*) of the resulting devices were about 8 μm and 500 nm unless others specify. The electrical properties were measured using semiconductor parameter analyzer (Keithley 4200 SCS) at room temperature under ambient conditions.

Statistical Analysis: Prior to analysis, all the EDS elemental maps were preprocessed by AZTech TEM EDS analyzing software (Oxford). All the electrical data were processed in Origin (OriginPro 2021, OriginProLab).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

artificial synapses, ferroelectric semiconductors, memtransistors, neuromorphic computing, two-dimensional nanomaterials

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